Novel Design Topology for Ultra Low Power Down Converters with Broadband on Chip Matching Network

Martin L. Schmatz, Urs Lott, *Member, IEEE*, Werner Baumberger, and Werner Baechtold

***Abstract*—A novel design topology for ultra low power receivers and down converters has been developed. Using this topology, a monolithic L-band down converter consisting of an input amplifier and a double balanced mixer has been implemented with a standard 0.7 μm GaAs-MESFET process. The circuit has a single ended 50 Ω input and differential outputs offering totally more than 40 dB voltage conversion gain at 1 GHz and 30 dB at 2 GHz. It is supplied by a single lithium cell and has a dc power consumption of less than 2.0 mW at 2.7 V. Through a more exact modeling of the parasitic capacitance of n-implanted resistors an improved agreement between measurement and simulation was achieved. Finally, the determination of the noise figure at a high impedance output from a 50 Ω measurement is presented.**

I. Introduction

PORTABLE COMMUNICATION SYSTEMS require down converters with very low power consumption. These parts of the system run at microwave frequencies and are therefore consuming a great portion of the receiver dc power. In order to fulfill the requirement of battery operation, a very low dc power consumption is a major design goal when developing such circuits [1].

A 50 Ω input impedance allows the receiver to be compatible with other high frequency blocks of the system. The matching circuits should be simple in order not to consume a lot of expensive chip area and may not introduce considerable loss thereby degrading the noise figure [2]. In conventional amplifiers, the input to the first active element is either a gate or a source of a transistor. Both of them have high impedances compared to 50 Ω, especially when the transistor has a small geometry and is operating at ultra low current levels. This makes broadband matching very difficult. Earlier approaches used wide transistors [4], [5] or high Q inductors [2] to overcome this problem. At a fixed dc power consumption, this costs gain, chip size and the transistors can not be biased for optimum noise figure [4], [5]. A matching network using many inductors is bound to have high insertion loss because of the parasitic resistance of integrated inductors.

Many design approaches use a separate amplifier and mixer chip with 50 Ω interface on every port. This consumes a lot of power and reduces conversion gain. For low IF output frequencies, a 50 Ω impedance level at the output is not necessary. Instead, an output impedance of some 2 kΩ would be convenient. The lowpass filter formed by this output resistance and the capacitance of an interchip connection (less than 5 pF) has a cutoff frequency above 15 MHz and lies clearly above typical IF frequencies. The cutoff frequency is even an order of magnitude higher when the input of the next stage is on the same chip.

One problem of high impedance interconnections is the measurement of noise figures of the single stages. Circuits running with very little current normally do not have any 50 Ω gain and they have a quite different frequency response when terminated into 50 Ω. Here, measurement through resistive output dividers is one possible solution.

Another problem of high on chip impedance levels arises from the fact that it is no longer possible to tune parasitic FET capacitances by means of inductors. The low Q of an integrated inductor is responsible for a rather low impedance of such a parallel resonant circuit. It lies well below the output impedance of a small transistor and becomes thereby the limiting factor for gain determination. This is the reason why we are bound to purely resistive loads in the different amplifying stages. These loads normally are formed by n-implanted resistors having some 1 k$\Omega/\square$. Unfortunately, they also do have a parasitic capacitance to ground. At L-band, these very little capacitances already do have an influence on the frequency response. This will be even more true for CMOS than for GaAs designs due to the better bulk material of GaAs. But even here, we can clearly measure the negative affect of the parasitic capacitances of the load resistors and they have to be modeled correctly.

All circuits presented in this paper were designed using the TriQuint QED/A process with GaAs E-(enhancement) and D-(depletion) FET. The gates of the E-FET are 0.7 μm long while the D-FET have a 1 μm long gate.

II. Circuit Design

The circuit presented in this work consists of a preamplifier with input matching network and with differential outputs, followed by a differential double balanced Gilbert cell mixer.

The preamplifier uses a novel input section consisting of a mixture between a common gate amplifier and a transimpedance amplifier (Fig. 1).

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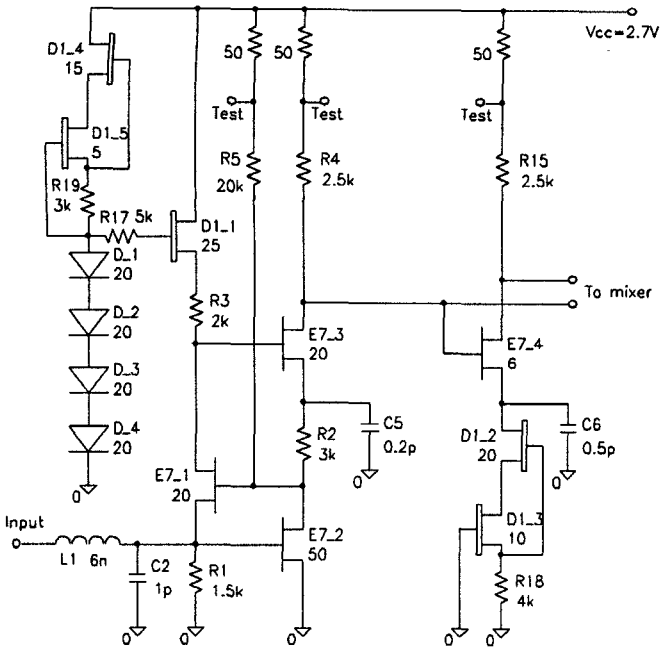

Fig. 1. Circuit schematic of the preamplifier.

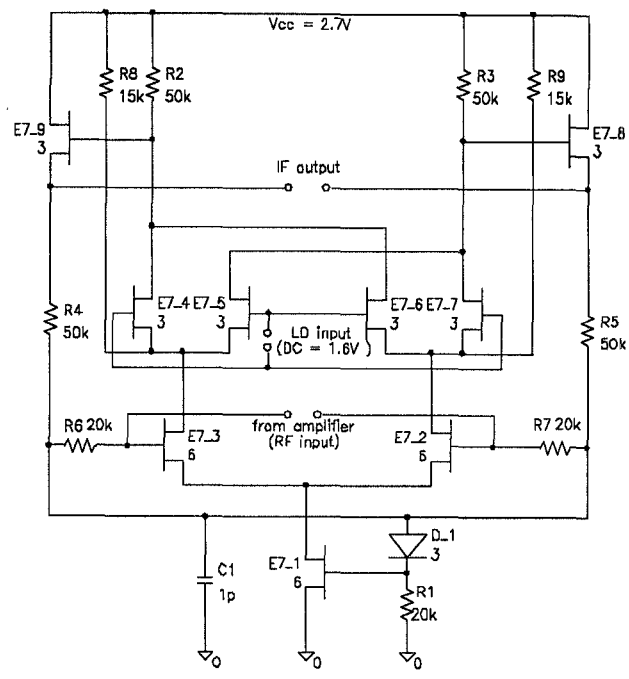

Fig. 2. Circuit schematic of mixer.

The FET E7_1 acts as feedback transistor driven from the common source transistor E7_2 and R2/R5. At the same time, it works as a common source transistor using the input impedance as series feedback. This topology results in high gain at very low dc power levels. Additionally, the input impedance measures only 200 Ω and can be matched to 50 Ω over a broad bandwidth with a single series inductor and a grounded capacitor having values compatible with integration.

The load of E7_1 is built around D1_1 and R5. This active/passive load configuration presents a high impedance and stabilizes the dc bias point of the circuit. Transistor E7_3 is power stacked on top of the input transistor using the capacitor C5 as ground. This allows a reuse of the current from transistor E7_2. The output of this additional common source amplifier is fed into the mixer directly and via the inverter transistor E7_4. The use of an inverter as a balun is very power efficient. With only about 80 μA of dc current, we achieve 6 dB of voltage gain. The phase deviation from 180 degrees is better than 10 degrees at 1.5 GHz. This deviation will affect the carrier suppression in the mixer and may be corrected by a good common mode suppression in the differential mixer input stage. The outputs are coupled to the mixer using two 200 fF capacitors. They have to be as small as possible in order to minimize the effect of stray capacitances.

The simulated voltage gain from the input to the differential output is more than 25 dB at 1.5 GHz.

The mixer (Fig. 2) uses a modified Gilbert cell [6] with feedback stabilization of the dc bias point. The resistors R8 and R9 inject current to the lower transistors and permit high passive load resistors with low voltage drop.

Additionally, this arrangement reduces the required LO drive level because of the low current level of the upper four transistors of the Gilbert cell. The high valued resistors R2 and R3 make the dc bias point of the circuit very sensitive to process tolerances. A small fluctuation in the current source transistor E7_1 will shift the dc voltages considerably. This is even more the case for the dc voltage at the LO ports. The low supply voltage does not allow for large deviations of bias points and a stabilization is therefore absolutely necessary. The output voltage of the IF signal is fed back to the current source transistor E7_1 via the resistor/diode combination R4/R5 and D_1. Additionally, the input bias for the lower transistors is generated with R6 and R7. High frequencies are filtered with the capacitor C1. This kind of stabilization allows a common mode voltage drift of the LO signal over a 0.3 V range causing a change of less than 1 dB in conversion gain. Supply voltage fluctuations are compensated as well.

The IF output is buffered by source followers in order to lower the output impedance to about 2 kΩ and to and make off chip filters feasible. The Gilbert helps to suppress the LO signal. This is important, when the IF signal is further processed with moderate additional filtering only: The chance of overloading the following stages due to unwanted signals is minimized.

The simulated voltage conversion gain of the mixer including buffers is 10 dB at frequencies around 1.5 GHz.

III. Determination of Parasitic Capacitances

From earlier low power designs [6] and [8], we noticed a difference between simulated and measured results. It was found that this difference could be minimized by adding a small capacitance to ground on every high impedance node of the circuit. A constant value of 13 fF was found to deliver better agreements between measurement and simulation, but there was still a notable difference.

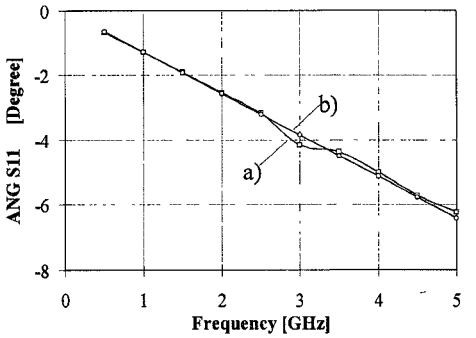

Fig. 3. Measurement a) and simulation b) of the input impedance (angle only) of an empty measurement structure.

A detailed analysis revealed two possible reasons for this difference:

1) The models base on measurements of 300 μm wide transistors may not be scaled down to very small transistor geometries. There could rest some constant offset resulting from cold capacitances when the scaling goes close to zero.
2) The resistors have a distributed parasitic capacitance large enough in order to have already an influence on the frequency response.

We developed two approaches to extract the parasitic capacitances. First, we integrated single test transistors with the same lateral geometry (i.e., gate fingers, contacts) but with different gate widths. Second, gain blocks with constant transistor geometries but different load resistors were implemented (Fig. 5).

For the determination of the equivalent circuit FET capacitances ($C_{gs}, C_{gd}, \ldots$), it is sufficient to know the parasitic capacitance of the wafer probe pads for deembeding. The pad inductances have small enough values not to show any influence at L-band. The pad capacitances were determined by two means: A measurement structure without an active device but with the final metalization layout was integrated and measured. This structure was additionally simulated using an electromagnetic simulator (EM/Sonnet). Measurement and simulation agree very well (Fig. 3). The corresponding capacitance is found to be 35 fF/pad for the applied layout.

Taking this pad capacitance into account, the parasitic capacitances of E-FET's with different widths but working at the same current density were extracted using a similar approach as in [9] and [10]. Fig. 4 shows the results from extractions for FET's with two gate fingers and a total gate width of 200 μm, 100 μm, 50 μm, 20 μm, 10 μm and 6 μm, respectively. It can be seen, that the capacitance scales to a zero value for a zero width transistor. This means, that the scaling of the transistor model is not responsible for the differences between circuit measurement and simulation.

The reason for the this differences will therefore lie in the parasitic capacitance of the n-implanted load resistors. In order to determine its value, the circuit shown in Fig. 5 was used. This configuration is compatible with wafer probing because the current levels of the two transistors may be set independently by external, coaxially fed bias voltages (bias

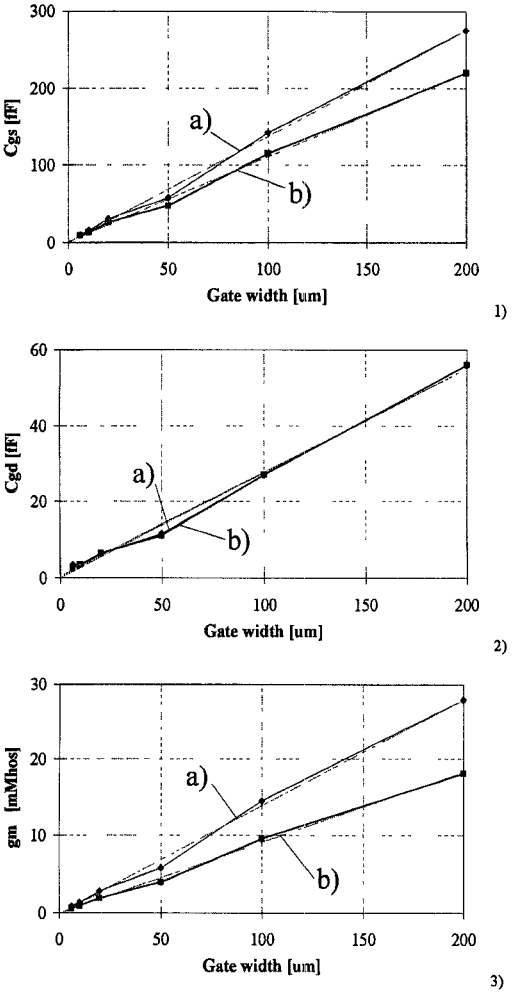

Fig. 4. Extracted equivalent circuit elements of an E-FET for different gate widths and current densities a) 15 mA/mm; b) 7.5 mA/mm 1) C_{gs}, 2) C_{gd}, 3) gm.

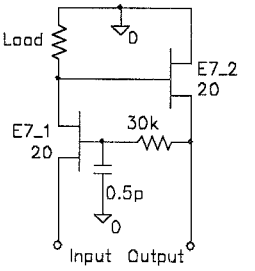

Fig. 5. Circuit schematic of the gain blocks.

tees of NWA). The values of the load resistors were chosen to be 3 kΩ, 5 kΩ, and 10 kΩ, respectively, while the transistors have a 20 μm wide gate.

For all three versions, the forward transmission coefficient was measured and its phase was compared with the simulation. It was noted that the measurement showed more phase shift than simulated. In order to account for this phenomenon, the simulation was repeated first with a concentrated capacitance added to the resistors, and second with the resistors modeled as RC distributed elements. Fig. 6 shows the differences between the measured phase shift and the phase shift obtained

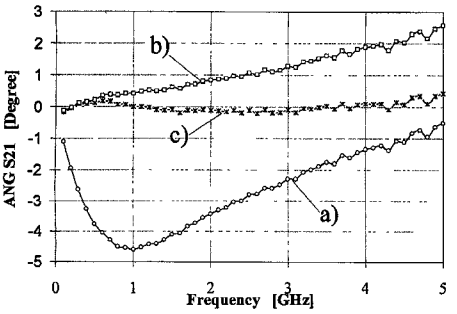

Fig. 6. Difference ($\varphi_{\text{meas}} - \varphi_{\text{simul}}$) between measurement and simulation of the gain block phase shift (10 kΩ load resistor); a) resistors without capacitance; b) resistors with concentrated capacitance; c) resistors with distributed capacitance.

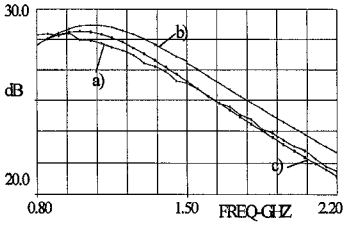

Fig. 7. Voltage gain of preamplifier: comparison between a) measurement; b) simulation without parasitic capacitance; c) simulation with distributed parasitic capacitance of resistors.

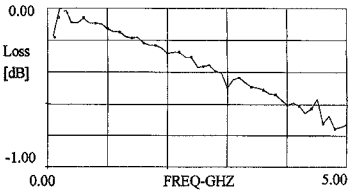

Fig. 8. Measured loss of input matching network (MAG calculated from S-parameters).

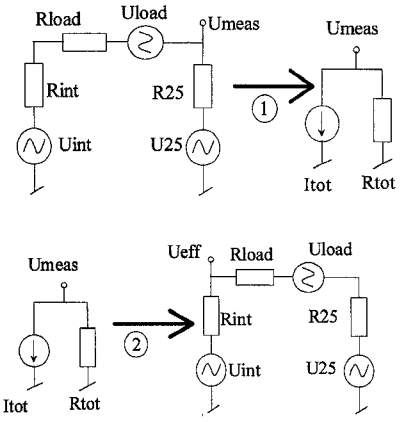

Fig. 9. Determination of the high impedance noise voltage U_{eff}.

by the tree simulations. It can be seen that for frequencies below 2 GHz, the parasitic capacitance may be modeled by a concentrated capacitance of 0.75 fF/kΩ, but that only the distributed RC model with normalized C' of 1.5 fF and R' of 1 kΩ shows differences in phase shift of less than 0.3 degrees up to 5 GHz. With no modeled capacitance, the error in the simulated phase shift is worse than 3 degree for L-band frequencies.

Fig. 7 shows the difference between measurement and simulation in the frequency response of the preamplifier with and without the parasitic capacitances taken into account. The simulation with the parasitic capacitances modeled as distributed elements shows very good agreement to the measurement.

IV. Input Matching Network

Modern down converter circuits should have on chip matching networks. This makes external matching PCB boards with large ε_r and thickness variations no longer necessary. A 50 Ω interface allows the circuit to be compatible with different standard antenna designs.

The on chip matching network must not introduce to much loss, because this will directly worsen the noise figure. It should also be broadband enough to allow operation on different channels.

The preamplifier presented in this work was matched to 50 Ω with one series inductance of 6 nH followed by a capacitance of 1 pF to ground. This configuration was integrated separately in a wafer probable form in order to determine its loss and impedance transformation.

Fig. 8 shows the measured insertion loss of the matching network. It is less than 0.3 dB for L-Band frequencies.

As mentioned earlier in this work, it is not possible to measure the noise figure at a high impedance interface directly. We therefore added a 50 Ω series resistor to every load resistor (Fig. 1). This allows the measurement of an amplitude scaled frequency response on every high impedance node with negligible influence on the circuit because of the high values of the load resistors compared to 50 Ω. The amplitudes of the actual signals may be easily calculated by using the formulas for resistive dividers. For the noise figure, things are not that easy because the resistive divider introduces noise itself. We also may not use the well known formulas for the noise calculation of cascaded amplifiers [11]: The load resistor is part of the amplifier and at the same time part of the output divider. We therefore developed a two stage procedure to extract the high impedance noise figure from the measured 50 Ω noise figure (Fig. 9).

In Fig. 9, R_{load} and U_{load} stand for the load resistor and its thermal noise voltage, R_{25} and U_{25} for the total measurement resistor and its thermal noise voltage, U_{int} is a combination of all internal noise sources of the amplifier and R_{int} is the output conductance of the output transistor (whose value will not contribute to the calculation if it is large enough), U_{meas} is the measured noise at the 50 Ω output and U_{eff} finally stands for the noise voltage at the high impedance output node we are interested in.

U_{int} is the only unknown noise source and may be calculated in a first step. This may be done by combining all noise voltages and resistors to a single noise current and resistor. Now, we are able to calculate in a second step the noise voltage U_{eff} at he high impedance node. Knowing this voltage, the small signal gain G of the amplifier and the thermal noise

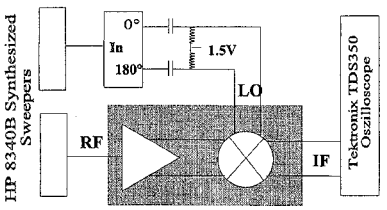

Fig. 10. Measurement setup.

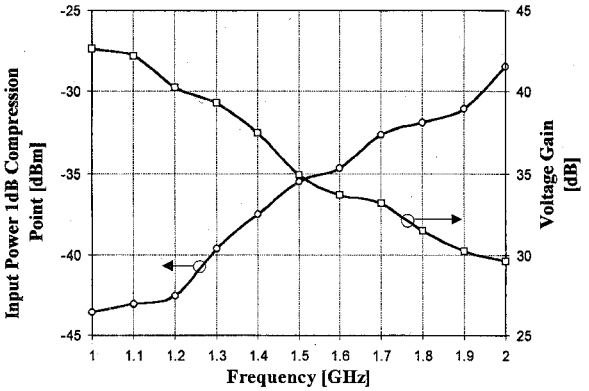

Fig. 11. Measured differential voltage conversion gain of the complete down converter and its 1 dB input compression point versus frequency ($f_{RF} = 1.5$ GHz; $f_{IF} = 2$ MHz).

voltage N of the 50 Ω input resistor, we can calculate the noise figure F

$$F = \frac{U_{\text{eff}}^2}{G \cdot N^2}.$$

V. Measured Results of the Realized Circuit

The realized chip measures 0.7 mm × 0.6 mm. The device is powered by a single 2.7 V supply with a low current consumption of 740 μA. It has a single ended input and differential outputs. All measurements were performed with a LO power of −2 dBm.

Several different parts of this circuit were integrated separately: First, the preamplifier alone with and without input matching circuit was realized. Additionally, the input matching inductor and capacitor were integrated in a wafer probe compatible form. Finally, a combination of mixer and preamplifier realized the complete down converter (Fig. 10).

Fig. 11 shows the measured gain and the 1 dB compression point for the input power vs. frequency. The conversion gain falls from more than 40 dB at frequencies around 1 GHz down to slightly less than 30 dB at 2 GHz. In parallel, the input power for a 1 dB compression in voltage conversion gain raises from −42 dBm to −28 dBm. This means that the maximum output voltage swing measures some 200 mV_{pp} on both IF outputs of the mixer.

Fig. 12 shows the two tone intermodulation performance of the down converter. Two 1.5 GHz RF signals with equal amplitude and 1 kHz offset were fed into the circuit and the intermodulation products were measured at one of the IF outputs. These measurements were performed into a 50 Ω load. This is possible, because the intermodulation products emerge

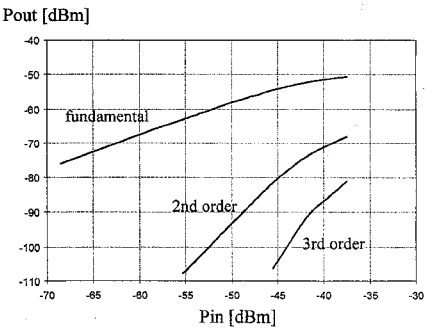

Fig. 12. Measured two tone intermodulation performance of the complete down contwerter.

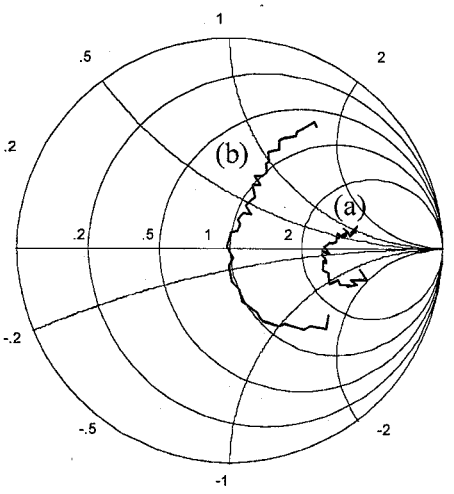

Fig. 13. Measured input impedance without (a) and with (b) input matching circuit.

not from the output buffers, but are generated in the earlier stages of the down converter. The 50 Ω load presented by the measurement setup explains the low values for the output power in Fig. 5. This down converter is not intended to drive 50 Ω loads. The second order input intercept point lies at −30 dBm input power, while the third order intercept point is at −28 dBm.

The difference between the input reflection with and without matching network is shown in Fig. 6. The input match is better than −15 dB for frequencies between 0.95 GHz and 1.45 GHz. This is more than 40% relative bandwidth ($\Delta f / f_{\text{center}}$). For an input match better than −10 dB the relative bandwidth is even more than 60% (0.85 GHz to 1.65 GHz). Its peak can be tuned for a desired frequency by varying the value of the input inductor and/or capacitor.

From a measured −14.8 dB 50 Ω gain and a 15.2 dB 50 Ω noise figure, we obtain a 5.5 dB noise figure at the 2.5 kΩ output of the amplifier using the previously described method. The single ended noise figure of the complete down converter was measured using a spectrum analyser and was determined to be 12 dB for a conversion from 1.5 GHz down to 2MHz. It is so high mainly due to the 1/f noise of the mixer at such a low IF frequency.

During the design of the circuit, noise performance was not optimized. The measured 5.5 dB noise figure of the

preamplifier may therefore not be considered to be the lowest possible noise figure achievable using this topology.

VI. Conclusion

An ultra low power L-band down converter with 50 Ω input, more than 35 dB voltage conversion gain and less than 2.0 mW dc power consumption is presented. It uses a novel design in the input stage of the preamplifier and a modified Gilbert cell. This new approach results in an input power match over a 40% relative bandwidth using an on chip matching network consisting of only one inductor and one capacitor. The bias point of the mixer is stabilized by dc feedback and allows therefore high load resistors and supply voltage variations between 2.7 V and 3.3 V.

The parasitic capacitance of n-implanted resistors was determined to measure 1.5 fF/kΩ and the influence of these parasitics on the presented circuit was investigated. These parasitics will be even larger on CMOS designs and further investigations in this direction should be made.

A method to calculate the noise figure on a high impedance output from a measurement on a 50 Ω resistive divider was developed.

The topology presented in this work is well suited for a very low power monolithic receiver front end for personal communications systems.

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